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(71) Applicant: **DIGITAL LIGHTWAVE, INC. [US/US]**
15550 Lightwave Drive, Clearwater, FL 33760 (US).

(72) Inventors: MYERS, Kenneth, T.; 2701 Country Woods Lane, Palm Harbor, FL 34683 (US). GARDNER, Douglas, J.; 2665 Beagle Path Way, Palm Harbor, FL 34683 (US).

(74) Agents: STEIN, Stefan, V. et al.; Holland & Knight, LLP, 400 North Ashley Drive, Suite 2300, Tampa, FL 33602 (US).

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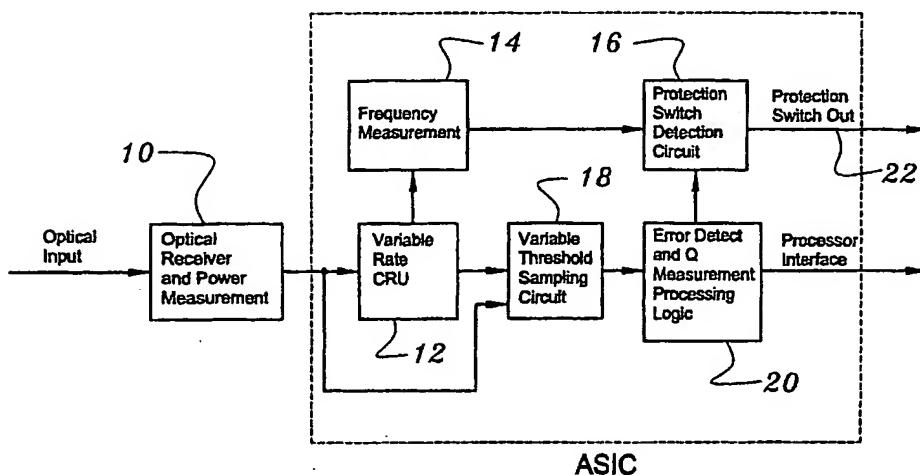
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(54) Title: PROTOCOL AND BIT RATE INDEPENDENT TEST SYSTEM



(57) Abstract: A protocol and bit rate independent test system includes a means for detecting bit errors on a digital communications channel regardless of format or rate. The system includes an optical receiver (10) for receiving an input signal, a clock recovery unit (12), a threshold-sampling circuit (18) and an error detection unit (20). The threshold sampling circuit (18) includes at least two threshold detectors for respective sampling points and phase adjustment units controlled by the output of the clock recovery unit (12). If the signal passes between a predetermined threshold, the error detection unit (20) generates a signal which is fed to a counter.

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PROTOCOL AND BIT RATE INDEPENDENT TEST SYSTEM

Cross Reference to Related Applications

This application is a utility application based upon and claiming priority of provisional application number 60/154,686, filed September 17, 1999 and application serial number 09/533,582, filed March 23, 2000, the disclosures of which are incorporated herein in their entirety by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a protocol and bit rate independent test system for digital communication systems. More particularly, this invention relates to systems that are able to detect bit errors on a digital communications channel regardless of format or rate.

Description of the Background Art

In digital communication systems, particularly dense wavelength division multiplexed (DWDM) optical systems, multiple signal formats may exist on the same communications link at different wavelengths. It is useful to be able to extract a signal and determine its health. Hence, there is a need to have a protocol independent and bit rate independent test capability that can (1) detect a single defective bit, (2) monitor the traffic error rate and (3) provide a protection switch signal within milliseconds of exceeding the error threshold condition, and to embed such a test head on every wavelength of the communications system, such as a DWDM system, so as to support such systems where the traffic on different

wavelength channels are different protocols and different bit rates. The channels will contain unknown protocols as purchased by the customers. In such a scenario, the customer can buy a wavelength of light and the service carrier does not control the rate or protocol of the traffic. This creates a difficult testing condition since the service provider needs a way to verify error free transmission, provide protection switching and location of the fault condition. The service provider therefore needs a test capability that is bit rate and protocol independent.

Heretofore it has been known that the performance of a communications link, such as a fiber optic link, known as Q factor measurement, is reflected by interpreting the eye pattern of the waveforms of a series of pulses. A typical eye pattern is depicted in Fig. 1. The optimal time for sampling the data signals and the optimal level (the threshold level) at which to distinguish between zeros and ones is the center of the eye. Further, it is known that the height of the central eye opening determines noise margin in receiver output, the width of the signal band at the corner of the eye depicts the jitter or variation in pulse timing in the system, the thickness of the signal line at top and bottom of the eye is proportional to noise and distortion in the receiver output, and transitions between top and bottom of the eye pattern show the rise and fall times of the signal that can be measured on the eye pattern. More complete descriptions of eye measurements (and of receivers and other components) can be found in the following references, the disclosures of each of which are incorporated by reference herein: Joseph C. Palais, *Third Edition Fiber Optic Communications*, Prentice Hall, Englewood Cliffs, N.J., 1992; John B.

Anderson, *Digital Transmission Engineering*, IEEE Press, Piscataway, N.J., 1999; Stephen B. Alexander *Optical Communication Receiver Design*, SPIE Optical Engineering Press, Bellingham, WA, 1997; Govind P. Agrawal *Fiber-Optic Communication Systems*, John Wiley & Sons, Inc, New York N.Y., 1997; Kaminow and Koch, *Optical Fiber Telecommunication IIIA*, Academic Press Limited, 1997; and Anderson and Lyle, Technique for Evaluating System Performance Using Q in Numerical Simulations Exhibiting Intersymbol Interference, *Electronics Letters*, Vol. 30, No. 1, Jan. 6, 1994. Unfortunately, Q measurements does not provide a real-time measurement or a single-bit error detection capability.

An object of this invention is to provide a bit rate and protocol independent test apparatus and method that can be embedded on every wavelength of a communications system such as a DWDM system.

Another object of this invention is to provide a bit rate and protocol independent capability that can (1) detect a single defective bit, (2) monitor the traffic error rate and (3) provide a protection switch signal within milliseconds of exceeding the error threshold condition of the communications system.

Another object of this invention is to provide an apparatus and method for conducting eye measurements to determine the Q factor.

The foregoing has outlined some of the pertinent objects of the invention. These objects should be construed to be merely illustrative of some of the more prominent features and applications of the intended invention. Many other beneficial results can be attained by applying the disclosed invention in a different

manner or modifying the invention within the scope of the disclosure. Accordingly, other objects and a fuller understanding of the invention may be had by referring to the summary of the invention and the detailed description of the preferred embodiment in addition to the scope of the invention defined by the claims taken in conjunction with the accompanying drawings.

SUMMARY OF THE INVENTION

For the purpose of summarizing this invention, this invention preferably comprises a discrete implementation or custom ASIC including the major components of a receiver, variable rate CRU (Clock Recovery Unit), and a very high speed threshold sampling module for various static or dynamic sampling points positioned in an array (two-dimensional or linear) that is able to instantaneously determine the shape of the eye of a digital communication system, and very high speed logic to process the data. This basic system meets the requirement and is the basis for a universal test set. In addition to bit error detection, it measures the frequency of the signal. Further enhancements includes creating oscilloscope eye diagrams and bit capture and post processing to identify the signal protocol by post processing. The preferred embodiment of the invention has particular application in optical communications systems, such as DWDM optical systems, employing an optical receiver; however, the invention may be incorporated into various other types of digital communication systems employing various other types of receivers without departing from the spirit and scope of this invention.

The foregoing has outlined rather broadly the more pertinent and important features of the present invention in order that the detailed description of the invention that follows may be better understood so that the present contribution to the art can be more fully appreciated. Additional features of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and the specific

embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the nature and objects of the invention, reference should be had to the following detailed description taken in connection with the accompanying drawing in which:

Fig. 1 is a exemplary eye diagram illustrating the various parameters thereof;

Fig. 2 is an overview block diagram of the bit rate and protocol independent test system invention;

Fig. 3 is a high-level block diagram of Fig. 1;

Fig. 4 is an exemplary eye diagram incorporating the invention; and

Fig. 5 is the anticipated initial implementation of Fig. 3.

Similar reference characters refer to similar parts throughout the several views of the drawings.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Fig. 2, the preferred apparatus of the invention comprises an optical receiver 10 that is preferably either PIN photodiode or avalanche photodiode (APD) based, with the former providing the lower cost. The invention also comprises a variable rate Clock Recovery Unit (CRU) 12 that is preferably phase locked loop (PLL) based to provide the desired flexibility. Frequency measurement 14 of the invention preferably comprises a high speed prescaler which drives a counter and provides a timebase to a protection switch detection circuit 16. A processor (not shown) is provided to measure the length of the divided down frequency to determine the line rate.

As described below in greater detail, the variable threshold sampling circuit 18 provides a plurality of threshold detectors. The output of these threshold detectors is sampled by the recovered clock. The thresholds are set as a percentage of peak eye amplitude and may be programmable. A minimum of two threshold detectors would be required to examine every bit. One threshold would be set in the upper area of the eye (i.e., 80% of peak) and the other set in the lower area of the eye (i.e., 20%). If the signal passes between the thresholds, it is considered an error. These are counted and may be read by a processor from the Error Detect and Q Measurement Processing Logic 20. Additional threshold sampling circuits with spread thresholds may be employed to provide further resolution and grading of each bit.

The protection switch detection circuit 16 compares the counted errors in a given timebase period with a programmable threshold. If exceeded, the protection switch output 22 goes active. This allows fast response to protection switch events with minimal software delays.

Referring now to Fig. 3, a more detailed description of the invention is presented as follows. The invention has an optical fiber input in which the incoming optical signal is fed to the optical receiver 10. The incoming optical power is measured by the power measurement block 10P. The receiver's output feeds the AGC input. The output of the AGC feeds multiple threshold adjustment blocks 18T (C and 1 through N) and the clock recovery unit 12. The clock recovery unit's clock is fed to multiple phase adjustment units 18P (C and 1 through N) that respectively control the clock feeding of multiple D Flip-Flops 18F (C and 1 through N) corresponding to the center data point C of the eye (see Fig. 4) and a plurality of arrayed data points (1 through N) positioned in an array about the other areas of the eye. The clock recovery unit also feeds the frequency measurement unit 14. The D Flip-Flops 18F are fed into an error detection circuit 20. The error detection circuit 20 feeds the error counter 20C. A high-speed control unit 16 controls all the threshold and phase adjustments. A high-speed information processing unit 16U processes all the incoming data. The protection switch unit 16S processes all the needed information and provides the protection switch signal 22. The interface unit provides an interface to the system controller 16C.

The anticipated first implementation of the invention is disclosed in

Fig. 5 that employs the CRU produced by Vitesse Semiconductor Corp. as disclosed in the article McCormack, Intelligent Data Recovery, Communication Systems Design, December, 1999, the disclosure of which is incorporated by reference herein, wherein the D Flip-Flops 18F and phase adjustment units 18P are "paired" and in which a error detection 20 and counter 20C is provided for each pair.

The theory of operation for each of the components is described as follows. The input channel is the analog path that converts the optical signal into a gain adjusted analog electrical signal. This channel includes the Clock Recovery Unit (CRU) which will extract the clock from the incoming data. The optical receiver preferably comprises a PIN receiver followed by an AGC into a variable rate Clock Recovery Unit (CRU). A PIN receiver and AGC is selected to provide a more linear analog channel. The CRU is flexible and provides continuous coverage from approximately 45 Mbit/sec to 2.7 Gbit/sec. Frequency measurement consists of a high speed pre-scaler that drives a counter. The frequency will be measured against a high quality clock source to derive the incoming frequency and also provide a timebase to the protection switch circuit.

The sampling block consists of a multiplicity of D Flip-Flops, such as in the anticipated first implementation, paired D Flip-Flops. There are separate controls of decision threshold and phase of the sampling clock. With control of the threshold and phase, the entire eye can be sampled or scanned across an array as shown in Fig. 4 (the number and positioning of the data points to be optimally determined). The following algorithm is provided as an example. The 1st step is to

find the optimum sampling position of the eye, typically the center C. After finding the optimum sampling position, one of the D Flip-Flops can be positioned at this location, hence the labeling "C". The other D Flip-Flop can now be used to scan around the eye to determine the margins, shape, and quality of the eye. The outputs of this sampling pair are fed to an error detection circuit that can determine bit value decision differences (decision errors) on a bit by bit real time basis.

Refer now to Fig. 4 for the example eye diagram used for the following description. Sampling point C indicates the center of the eye and point 1 indicates the point of one of the D Flip-Flop pairs. The sample point of this pair C and 1 (as well as the other individual points) can be moved around the eye independently. For example, in Fig. 5, with point C being the center of the eye, point 1 can be moved around to obtain information from the eye or left static to provide real time error information. As point 1 moves into this boundary of the eye, decision errors will start to occur. Combined with other points that may be dynamically moved around or made to remain static, many other decision errors will start to occur. By statistically processing the decision errors, eye profiling and Q measurements can be made. By fixing the relative position of the points, algorithms can be developed that will allow for accurate monitoring of the traffic BER. Importantly, the flexibility of the apparatus and method of the invention allows adaptation to the particular implementation with its inherent characteristics (i.e., satellite or microwave).

The control and processing block controls of all the system adjustments and access to all the data. This block provides all real time control and data

processing. Processing of the controls and error detect circuitry allows for Q measurements and BER analysis. Processing of the errors and clock rate provides a protection switch signal. The programmable nature of the invention allows the service provider to set the parameters to achieve the confidence level required by the customer before generating a protection switch signal. The bit rate affects the time and confidence level obtainable in a given time period. This trade-off is to be optimized with respect to the protection switch time.

Optical Receiver Block should support 1310 nm band and 1550 nm band input optical range and a pin receiver. It is noted that an APD receiver may be required to provide input sensitivity or a PIN receiver may be calibrated to mimic the APD's performance, thus saving the cost of an APD.

Optical Receiver Power Measurement measures the receiver optical power and the optical power from approximately 0 dBm to -35 dBm.

Automatic Gain Control (AGC) Block provides approximately 40 dB of gain range and approximately 20 mV of input sensitivity.

Threshold Adjustment Block provides approximately 64 adjustable threshold steps.

Continuous Clock Recovery Block supports input data rates from approximately 45 Mbit/sec to 2.7 Gbit/sec.

Frequency Measurement Block provides bit rate measurement, a high speed pre-scaler which drives a counter and a high quality clock reference to measure the incoming frequency against.

Phase Adjust Block provides approximately 64 adjustable phase steps.

D Flip-Flop Block provides data sampling and supports threshold adjustments and clock phase adjustments.

Error Detection Block supports error detection by comparing the D Flip-Flops outputs.

Error Counter Block supports error counting of the error detection block.

High Speed Control Block provides control of the threshold adjustment block, the phase adjustment block, the clock recovery block and the AGC block.

High Speed Information Processing Block retrieves data from the AGC block, from the threshold adjustment block, from the phase adjustment block and from the error counter block.

The present disclosure includes that contained in the appended claims, as well as that of the foregoing description. Although this invention has been described in its preferred form with a certain degree of particularity, it is understood that the present disclosure of the preferred form has been made only by way of example and that numerous changes in the details of construction and the combination and arrangement of parts may be resorted to without departing from the spirit and scope of the invention.

Now that the invention has been described,

WHAT IS CLAIMED IS:

1. A protocol and bit rate independent test system including means for detecting bit errors on a digital communications channel regardless of format or rate, comprising in combination:

- a receiver for receiving an input;
- a clock recovery unit;
- a threshold sampling circuit for providing at least two threshold detectors for respective two sampling points, the output of which are sampled by the recovered clock and if the signal passes between the thresholds, an error signal is generated and counted.

2. The protocol and bit rate independent test system as set forth in Claim 1, wherein the sampling points comprise static sampling points.

3. The protocol and bit rate independent test system as set forth in Claim 1, wherein the sampling points comprise dynamic sampling points.

4. The protocol and bit rate independent test system as set forth in Claim 1, wherein the sampling points comprise static and dynamic sampling points.

5. The protocol and bit rate independent test system as set forth in Claim 1, wherein the sampling points are positioned in an array about an eye measurement.

6. The protocol and bit rate independent test system as set forth in Claim 5, wherein the array comprises a linear array.

7. The protocol and bit rate independent test system as set forth in Claim 5, wherein the array comprises a two-dimensional array.

8. The protocol and bit rate independent test system as set forth in Claim 1, wherein said clock recovery unit comprises a variable rate clock recovery unit.

9. The protocol and bit rate independent test system as set forth in Claim 1, wherein said receiver comprises an optical receiver and wherein said input comprises an optical input.

10. The protocol and bit rate independent test system as set forth in Claim 9, wherein the optical receiver is PIN photodiode based.

11. The protocol and bit rate independent test system as set forth in Claim 9, wherein the optical receiver is avalanche photodiode based.

12. The protocol and bit rate independent test system as set forth in Claim 1, further including frequency measurement including a high speed prescaler which drives a counter and provides a timebase to a protection switch detection circuit.

13. The protocol and bit rate independent test system as set forth in Claim 1, wherein said threshold sampling circuit comprises a variable threshold sampling circuit.

14. The protocol and bit rate independent test system as set forth in Claim 1, further including an error detect and Q measurement processing logic for reading the error signals

15. The protocol and bit rate independent test system as set forth in Claim 12, further including a protection switch detection circuit for comparing the

counted errors in a given timebase period with a programmable threshold and upon exceeding the threshold, for producing an active protection switch output.

16. The protocol and bit rate independent test system as set forth in Claim 1, further including a jitter measurement processing logic.

17. A protocol and bit rate independent test system method for detecting bit errors on a digital communications channel regardless of format or rate, comprising in combination:

receiving an input signal;

recovering the clock from the input signal;

sampling at least two sampling thresholds from the input signal; and

producing an error signal if the input signal passes between the thresholds.

18. The method as set forth in Claim 17, wherein the sampling points comprise static sampling points.

19. The method as set forth in Claim 17, wherein the sampling points comprise dynamic sampling points.

20. The method as set forth in Claim 17, wherein the sampling points comprise static and dynamic sampling points.

21. The method as set forth in Claim 17, wherein the sampling points are positioned in an array about an eye measurement.

22. The method as set forth in Claim 21, wherein the array comprises a linear array.

23. The method as set forth in Claim 21, wherein the array comprises a two-dimensional array.

24. The method as set forth in Claim 17, wherein the step of recovering the clock from the input signal comprises the step of recovering the clock from the input signal at a variable rate.

25. The method as set forth in Claim 17, wherein the step of receiving a signal input comprises the step of receiving an optical signal input.

26. The method as set forth in Claim 25, wherein the step of receiving the optical signal input employs an optical receiver.

27. The method as set forth in Claim 26, wherein the optical receiver is PIN photodiode based.

28. The method as set forth in Claim 27, wherein the optical receiver is avalanche photodiode based.

29. The method as set forth in Claim 17, further including the step of measuring the bit rate to provide a timebase to a protection switch detection circuit.

30. The method as set forth in Claim 17, wherein the step of sampling at least two sampling thresholds from the input signal comprises the step of sampling at least two variable sampling thresholds.

31. The method as set forth in Claim 17, further including the step of reading the error signals.

32. The method as set forth in Claim 31, wherein the step of reading the error signals employs an error detect and Q measurement processing logic.

33. The method as set forth in Claim 17, further including the step of comparing the counted errors in a given timebase period with a programmable threshold and upon exceeding the threshold, producing an active protection switch output.

34. The method as set forth in Claim 17, further including the step of measuring jitter.

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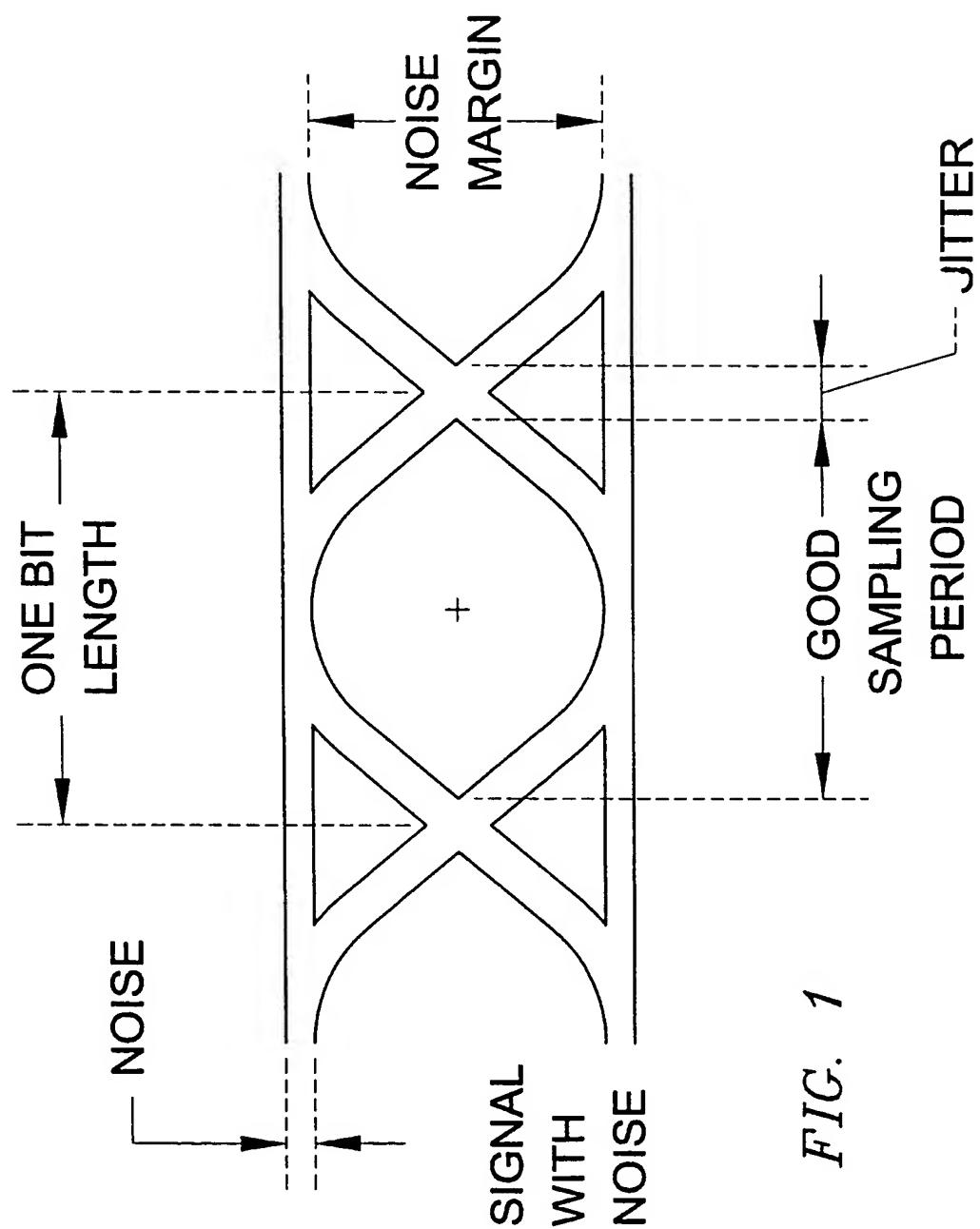


FIG. 1

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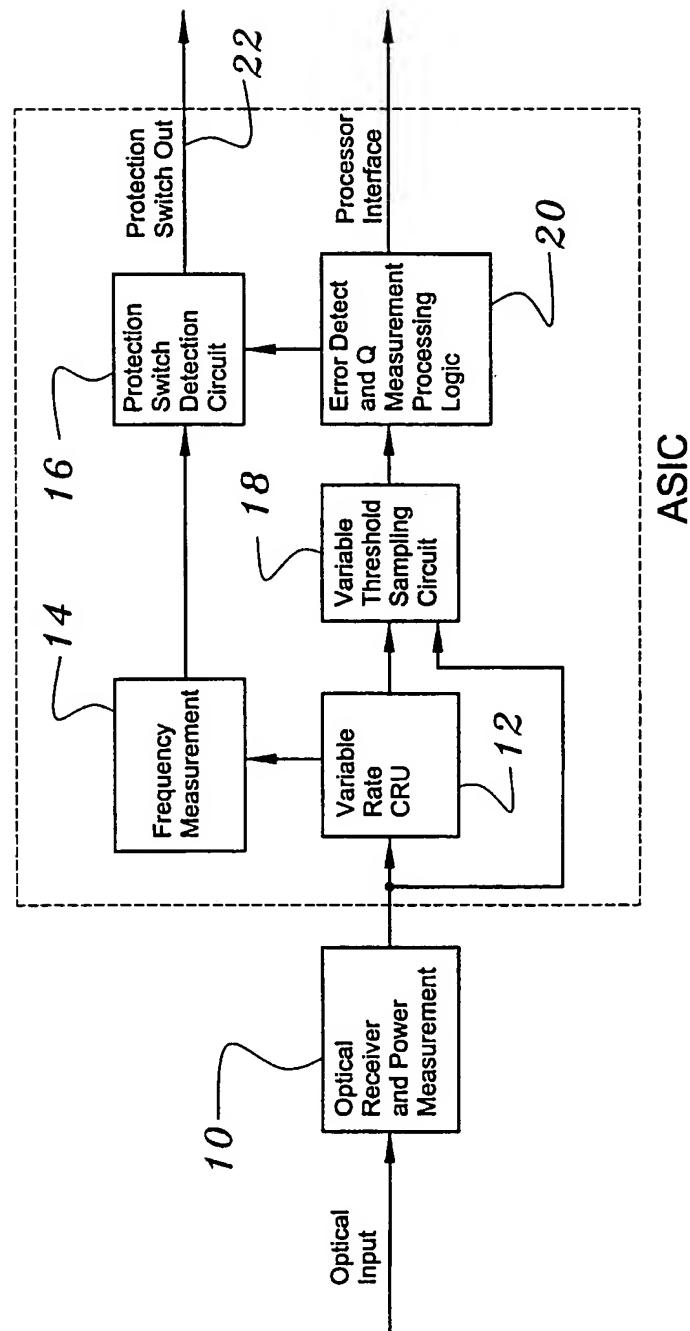


FIG. 2

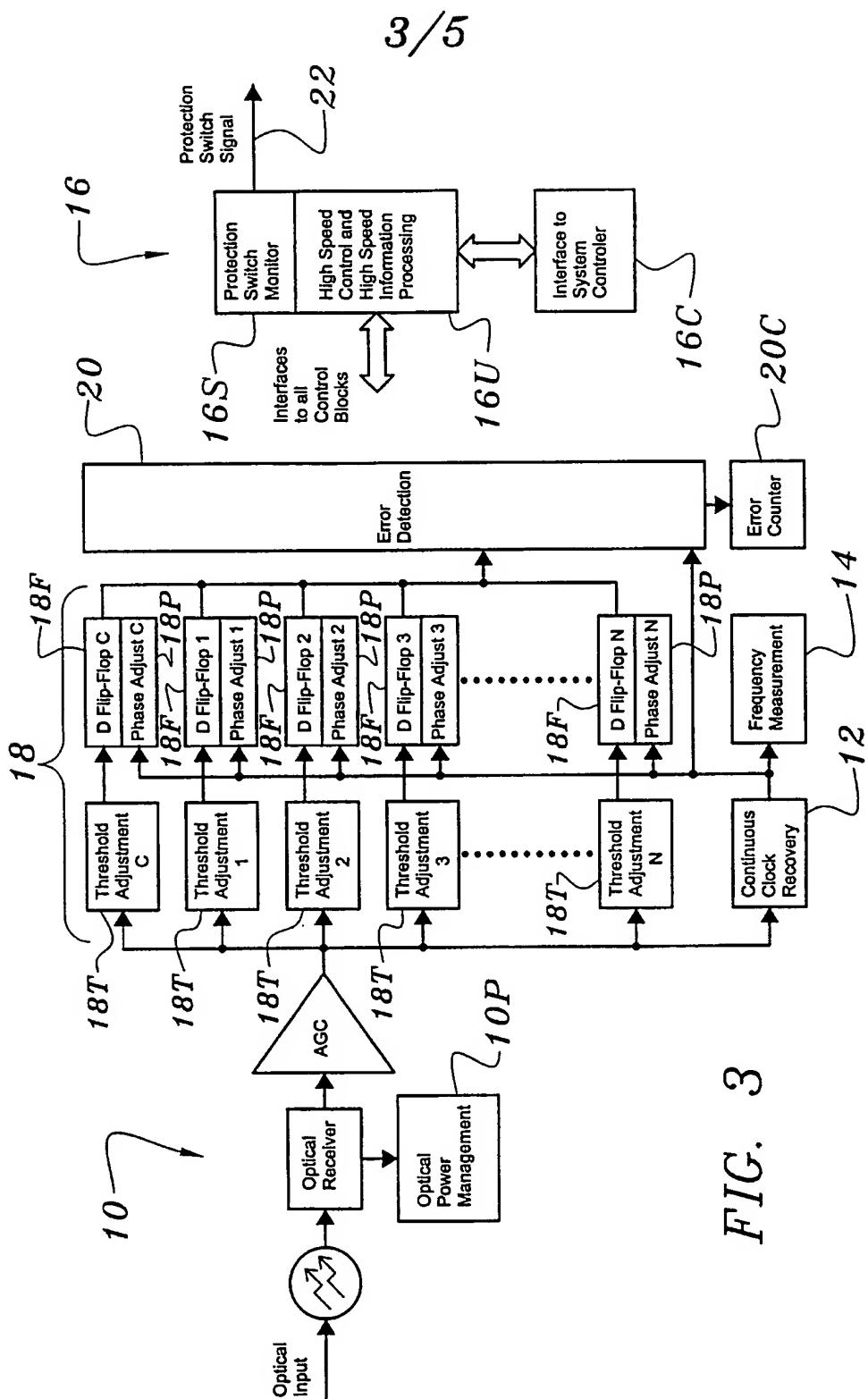


FIG. 3

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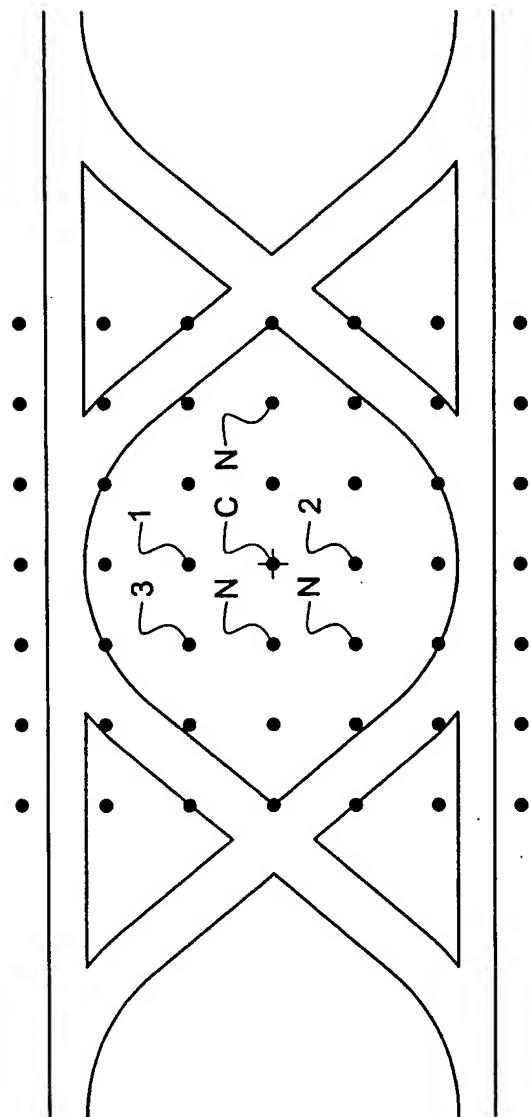


FIG. 4

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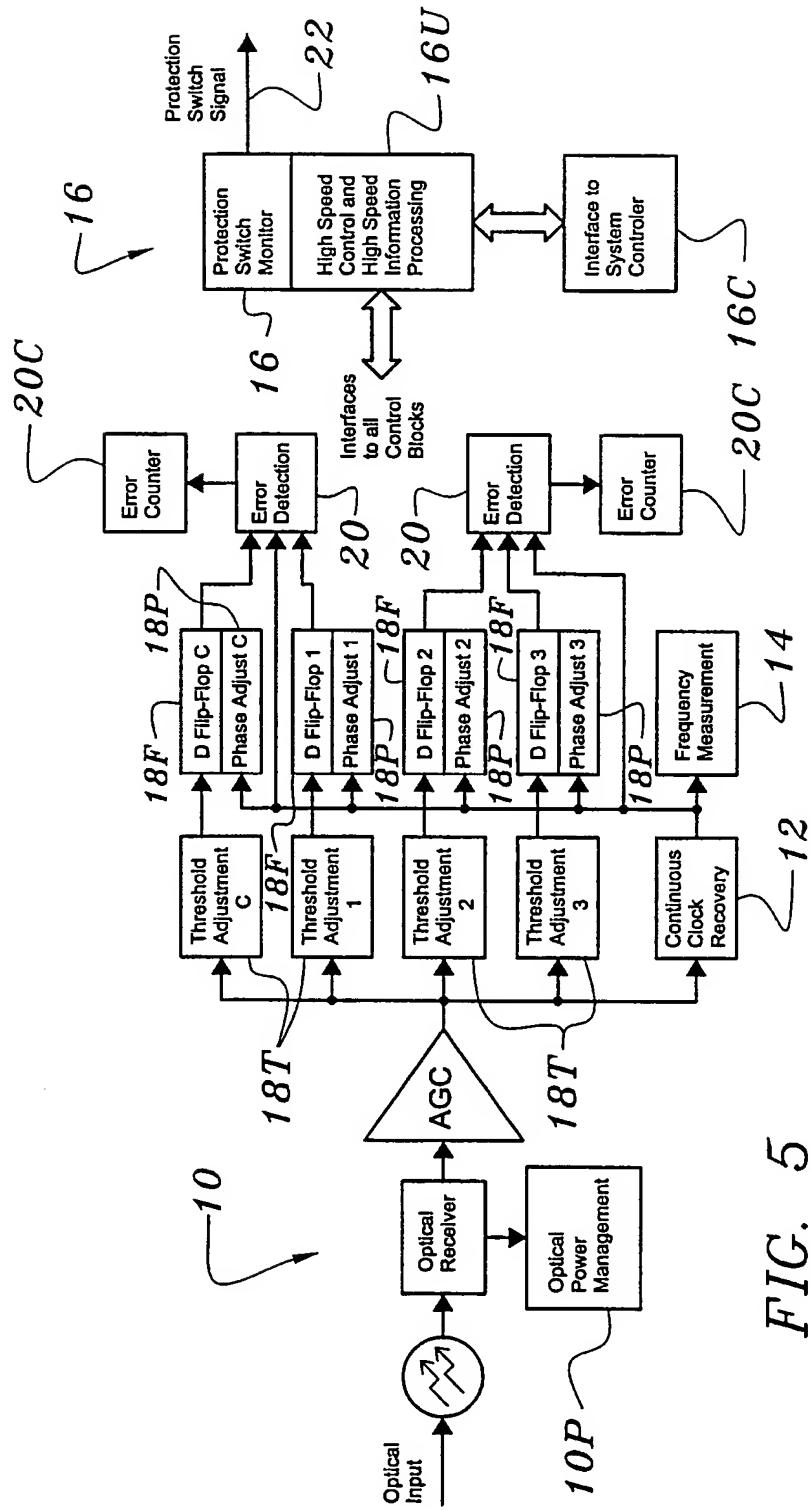


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No

PCT US00-25351

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G06F 11/00; H03M 13/00; H04B 17/00, 10/08, 10/04; H04L 07/00

US CL : 714:704, 708, 709; 375/371, 224; 359/110, 180

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 714:704, 708, 709; 375/371, 224; 359/110, 180

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

IEEE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST & WEST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,633,465 A (FITCH et al) 30 December 1986, fig. 8; col. 1, lines 14-22 and 52-60; claims 1 and 2; Abstract; col.4, lines 8-17.	1-4, 13, 17-20, 30
X	US 5,333,147 A (NOHARA et al) 26 July 1994, col. 4, lines 46-67; col. 5, lines 40-63; col. 8, lines 1-10; col. 6, lines 62-67; col. 7, lines 1-15; claim 17 and fig. 4.	1, 5-8, 17, 21-24
X	US 5,617,238 A (BOGDAN et al) 01 April 1997, col. 8, lines 1-19; col. 3, lines 39-63; col. 9, lines 26-58; col.4, Summary; col. 10, step 15; col. 11, step 19.	1, 9, 10, 14, 17, 25-27, 31, 32
X,P	US 6,084,931 A (POWELL, II et al) 04 July 2000, col. 3, lines ; col. 3, lines 45-50; col. 10, lines 13-26; col. 9, lines 6-46; col. 13, lines 62-67; fig. 1.	1, 12, 15-17, 29, 33, 34

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

International application No PCT US00 25351
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	US 4,809,306 A (SOMER) 28 February 1989, col. 2, lines 41-67.	8, 24
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X	US 5,644,417 A (AULET et al) 01 July 1997, col. 3, lines 39-63; col. 4, lines 1-24; figure 5; col. 10, step 15; col. 16 step 19.	1, 9, 10, 14, 16, 17, 25-27, 31, 32, 34
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Y	US 5,774,242 A (O'SULLIVAN et al) 30 June 1998, figure 1, 3, 4 and 5; col. 2, lines 44-67; col. 4, lines 12-24; col. 4, lines 65-67; col. 5, lines 1-67; and formulas in col. 6; col. 1, lines 62-67.	1-7, 9-11, 17-23, 25-28
Y	US 5,870,211 A (YOSHIDA) 09 February 1999, col. 2, Summary; col. 4, lines 40-53.	2-7, 9-11, 18-23, 25-28